Review of device matching improvement methods in integrated circuits

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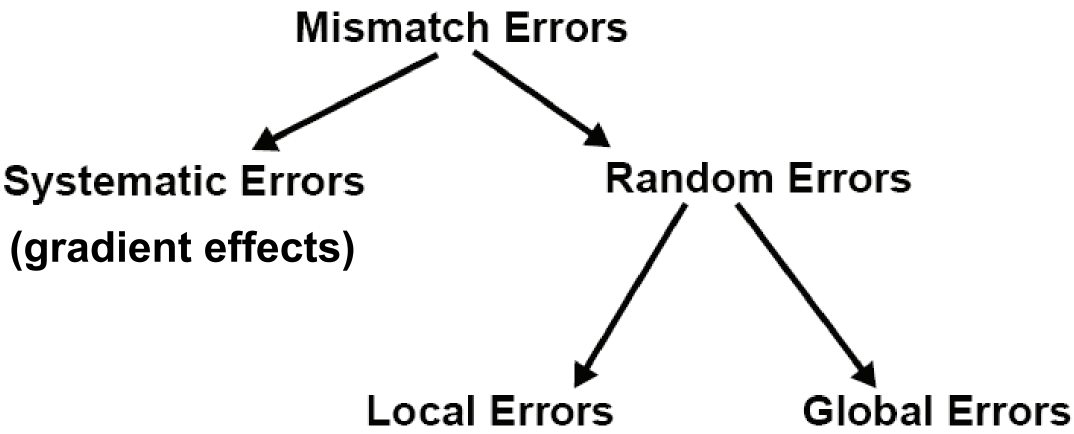
- With the advances in technology leading to smaller feature sizes and more stringent design constraints, device mismatch considerations are becoming increasingly important.
- Methods of modeling of random and systematic mismatch will be reviewed.
- The most prospective layout techniques for both linear and nonlinear gradient cancellation will be shown.

Definition



Mismatch Errors

Systematic Errors (gradient effects)

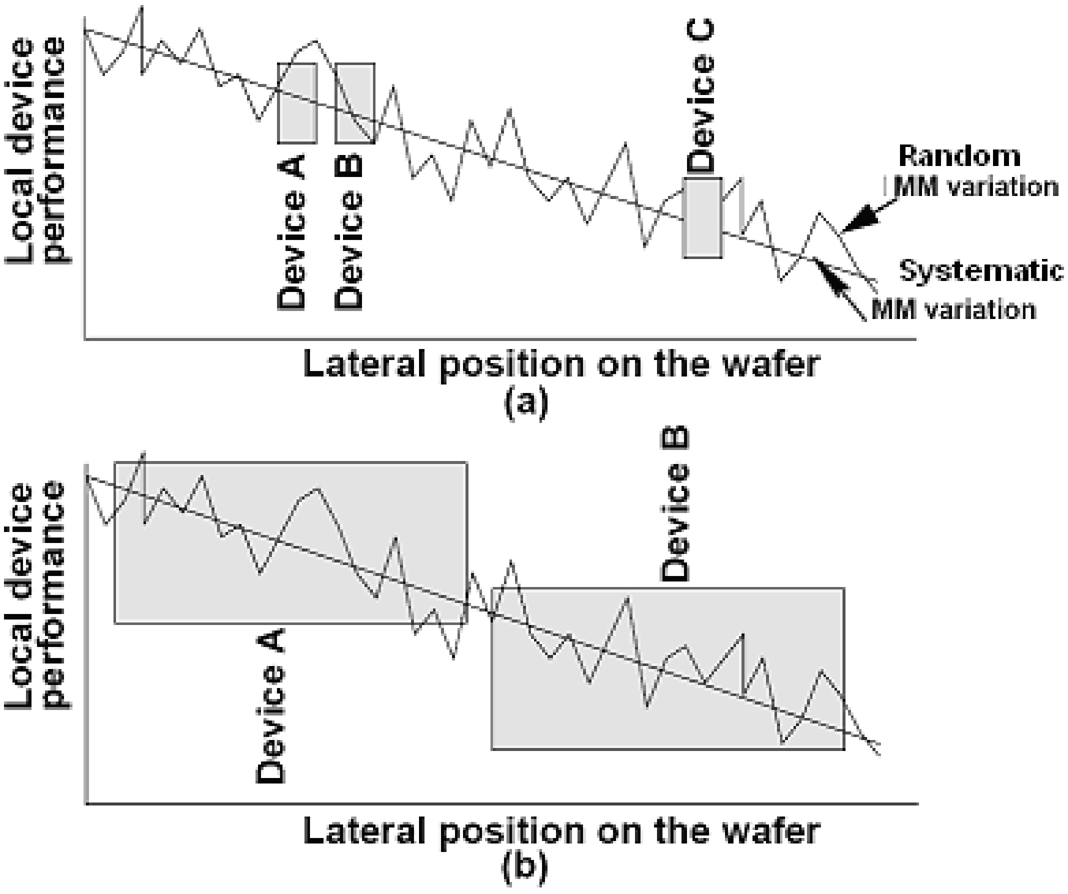
Random Errors

Local Errors

Global Errors

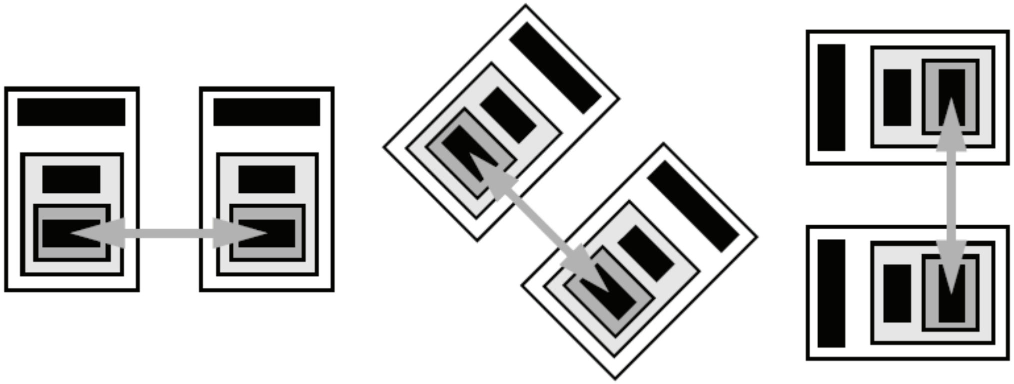
- **<u>Systematic mismatch</u>** is that part of the total mismatch where a deterministic trend can be observed in the mismatch values of the various transistors. It can be precisely predicted, given the process gradients.
- **<u>Random mismatch</u>** represents that portion of the mismatch which is stochastic and hence cannot be predicted.

Graphical depiction of random and systematic variations



Layout considerations that affect matching:

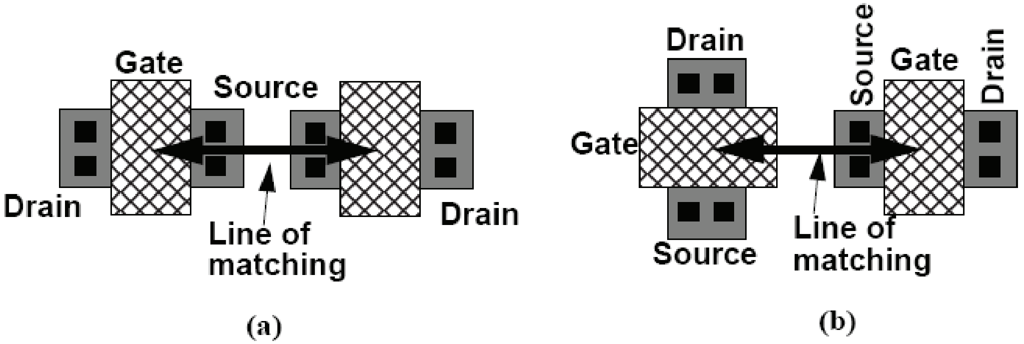
- **Geometry** - the **random** component of mismatch improves with increasing geometry.
- **Proximity** - physical separation distance between matched devices, the center-to-center spacing of the devices.
- **Matching orientation** - the orientation of the line *("line of matching")* that connects the center of the device in a matched pair(s). Matching orientation is measured in degrees with reference to the wafer flat or notch.



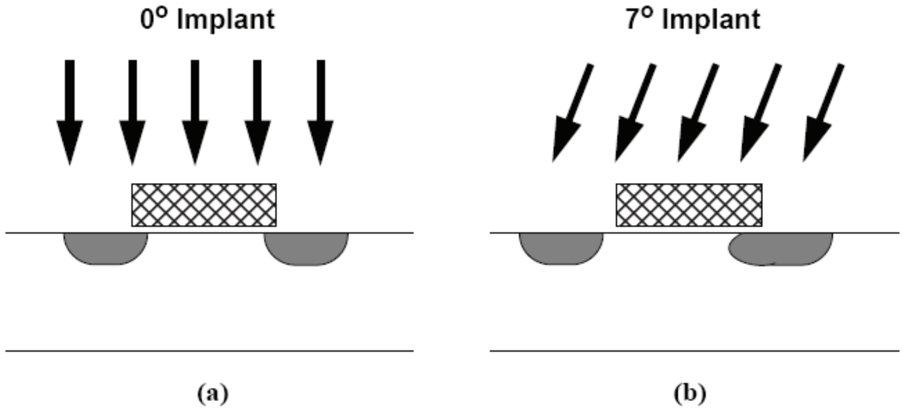
Variations on matching orientation. The arrows represent the "line of matching".

Layout considerations that affect matching (continued):

- **<u>Device orientation</u>** - the orientation of each device in a matching pair with respect to the wafer flat or notch. Device orientation can be important for mismatch for ***two reasons***:
    1. Carrier mobility varies with orientation;
    2. Ion implantation (I/I) angle to the wafer surface may vary. For better control of the ion implantation depth and spread in the depth direction, wafers are implanted with a 7^{o} tilt on the wafer, which minimizes the channelling effect. This angled implant will create a *<u>shadowing effect</u>*, the source/drain regions will be symmetric if the implant angle is 0^{o} or if the 7^{o} implant angle is along with gate polysilicon.



Variations of device orientation



The effect of ion implantation shadowing in (b) versus a 0^{o} implant in (a).

Models for analysis of matching properties

Basic models of random mismatch analysis

- The drain current mismatch in the saturation region is given by (model of Lakshmikumar) :

$$\frac{\sigma_{Id}^2}{Id^2} = \frac{\sigma_\beta^2}{\beta^2} + 4\frac{\sigma_{V_T}^2}{(V_{GS} - V_T)^2}$$

- Variance of parameter *ΔP* between two rectangular devices is given by (model of Pelgrom):

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2 .$$

where

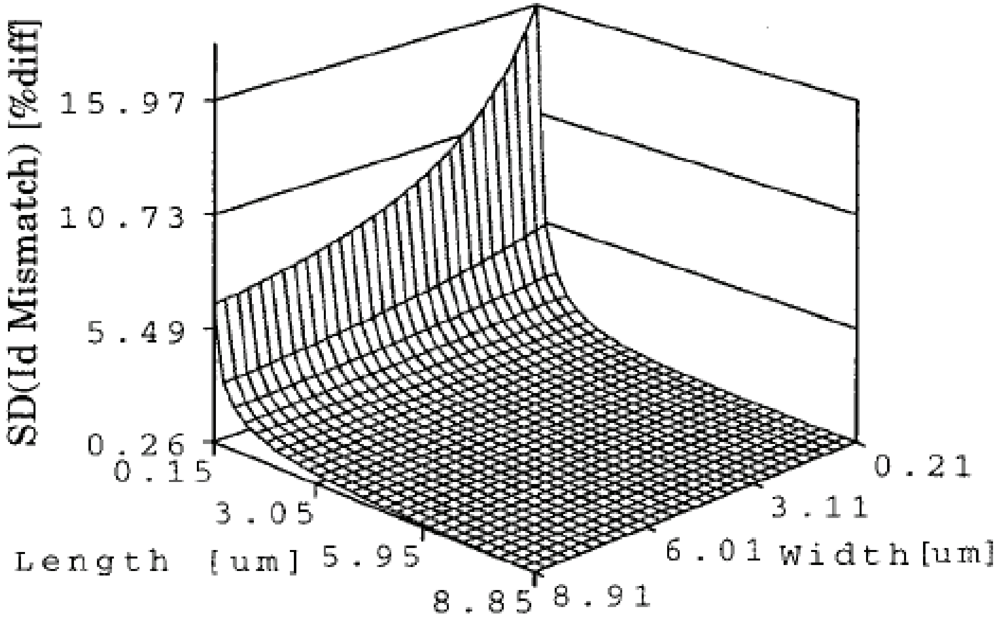
β – current factor,

V_T – threshold voltage,

A_P - area proportionality constant for parameter *P*,

S_P - variation of parameter *P* with the spacing D_x.

Application of random mismatch model



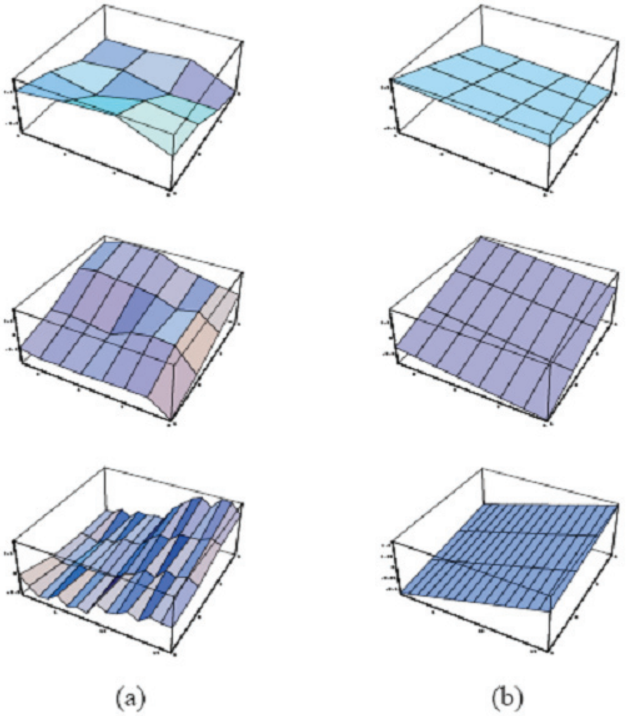
Three-dimensional (3-D) plot of I_d mismatch versus L and W for an nMOS current mirror, $I_{\text{ref}} = 10\ \mu$A, 0.13-μm CMOS technology.

Increase in ***L*** is more effective for random mismatch reduction than increase in ***W***:

- *L increases* => intrinsic mismatch decreases, ($V_{GS} – V_T$) increases to supply the same reference current. This leads to decrease in σId.
- *W increases* => intrinsic mismatch component decreases, but ($V_{GS} – V_T$) decreases. These two effects offset each other, and can give rise to little or no decrease in σId.

Considering random and systematic mismatch in models

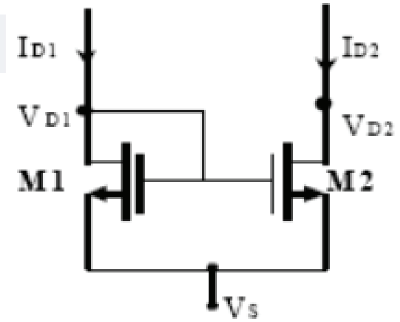
- Total mismatch should be characterized as a **sum of systematic and random components**.
- Systematic component usually models linear gradient across the die:



(a) 3-D plots of actual intra-die mismatch (nonlinear gradient).
(b) Systematic mismatch approximated by a linear gradient

Basic models of systematic mismatch analysis

(linear gradient)

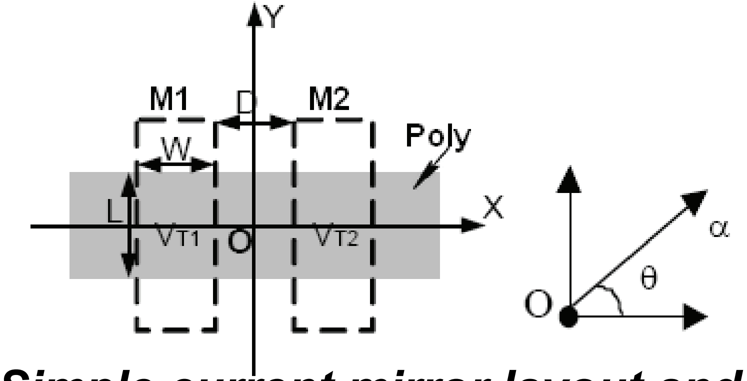


Basic current mirror

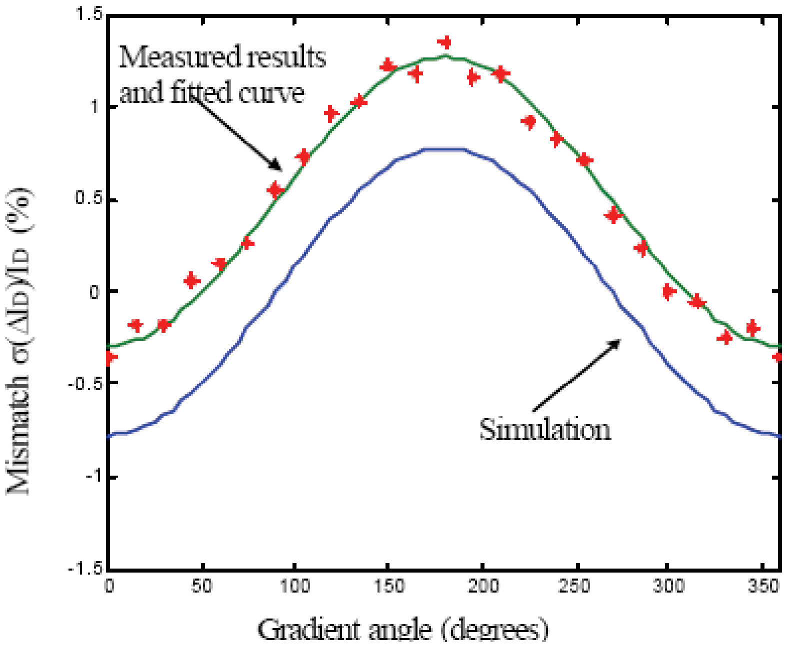
$$V_{T1} = V_{TN} + \left(-D/2 - W/2, 0\right)\bullet\left(\alpha\cos\theta, \alpha\sin\theta\right)$$
$$= V_{TN} - \alpha\left(\frac{W}{2} + \frac{D}{2}\right)\cos\theta$$
$$V_{T2} = V_{TN} + \left(D/2 + W/2, 0\right)\bullet\left(\alpha\cos\theta, \alpha\sin\theta\right)$$
$$= V_{TN} + \alpha\left(\frac{W}{2} + \frac{D}{2}\right)\cos\theta$$

$$I_D = \frac{1}{2} C_{OX} \mu_N \left(\frac{W}{L}\right)\left(V_{GS} - V_T\right)^2$$

$$\boxed{Mismatch = \frac{I_{D2} - I_{D1}}{I_{D1}} x100\ \%}$$



Simple current mirror layout and Linear gradient model



Basic models of systematic mismatch analysis

(nonlinear gradient)

Generally, a parameter that has up to *n*th-order gradient components can be modeled as:

$$p_n(x, y) = \sum_{j=1}^{n} G_j(x, y) + C \, ,$$

where

$$G_j(x, y) = \sum_{k=0}^{j} g_{k,j-k} x^k y^{j-k}$$

is the j^{th}-order component. $g_{k,j-k}$-s are the j^{th}-order coefficients.

Considering mismatch among devices in multiple lots

Variations of any model parameter γ can be expressed as:

$$\gamma(x, y)=\gamma_{NOM}+\gamma_{PROC}+\gamma_{WAFER}+\gamma_{DIE}+\gamma_{SYS}(x, y)+\gamma_{RAN}(x, y)$$

where

- x,y – position on the die
- γ_{NOM} – nominal value of the model parameter
- Other variables are random parameters:
  - γ_{PROC} - variation lot to lot;
  - γ_{WAFER} - variation wafer to wafer in a lot;
  - γ_{DIE} - variation die to die on a wafer;
  - γ_{SYS} – systematic variation location to location on a die, this parameter is position dependent;
  - γ_{RAN} – random variation at the position (x,y);

For devices in close proximity to each other on a die γ_{PROC}, γ_{WAFER}, γ_{DIE} are nearly constant, so most researches focus on last 2 terms.

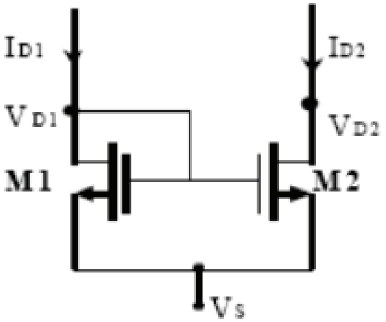
Models for analysis of matching properties: Conclusion

- Random mismatch has stronger dependence on L than on W.
- The total transistor mismatch should be modeled as the superposition of random mismatch and systematic mismatch.
- Systematic mismatch can be modeled as a linear gradient across the die.

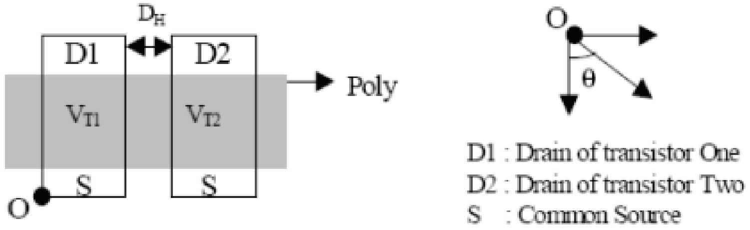
Layout techniques for improved matching

Reduction of mismatch (linear gradient consideration)

Most widely used layout techniques

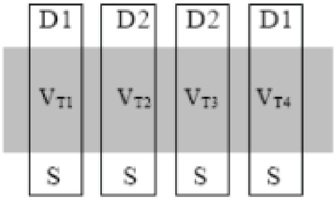


Basic current mirror

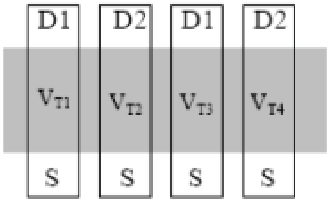


D1 : Drain of transistor One
D2 : Drain of transistor Two
S : Common Source

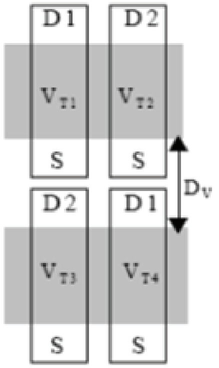
(a) Simple Technique



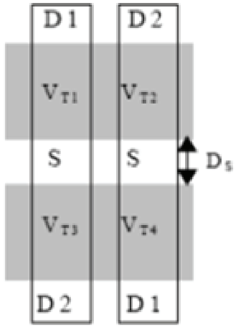
(b) Interdigitized Type I



(c) Interdigitized Type II



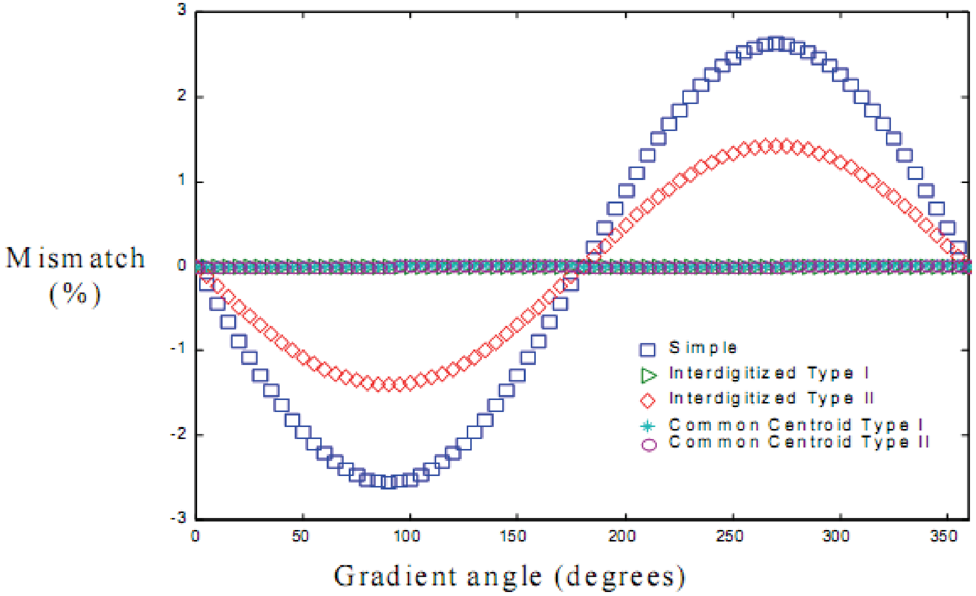
(d) Common Centroid Type I

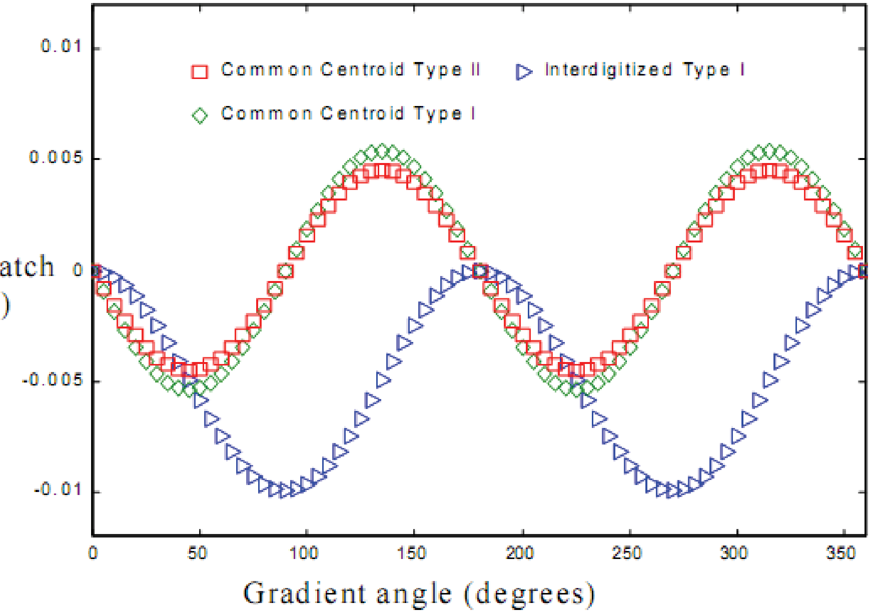


(e) Common Centroid Type II

Reduction of mismatch (linear gradient consideration)

Simulations of most widely used layout techniques

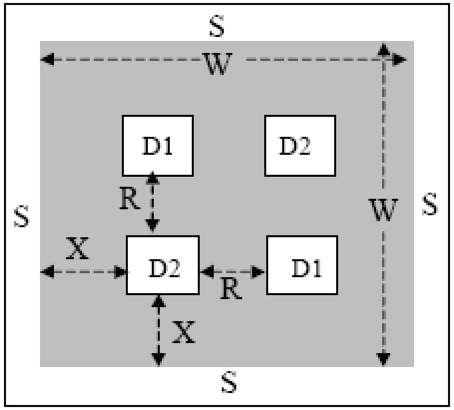


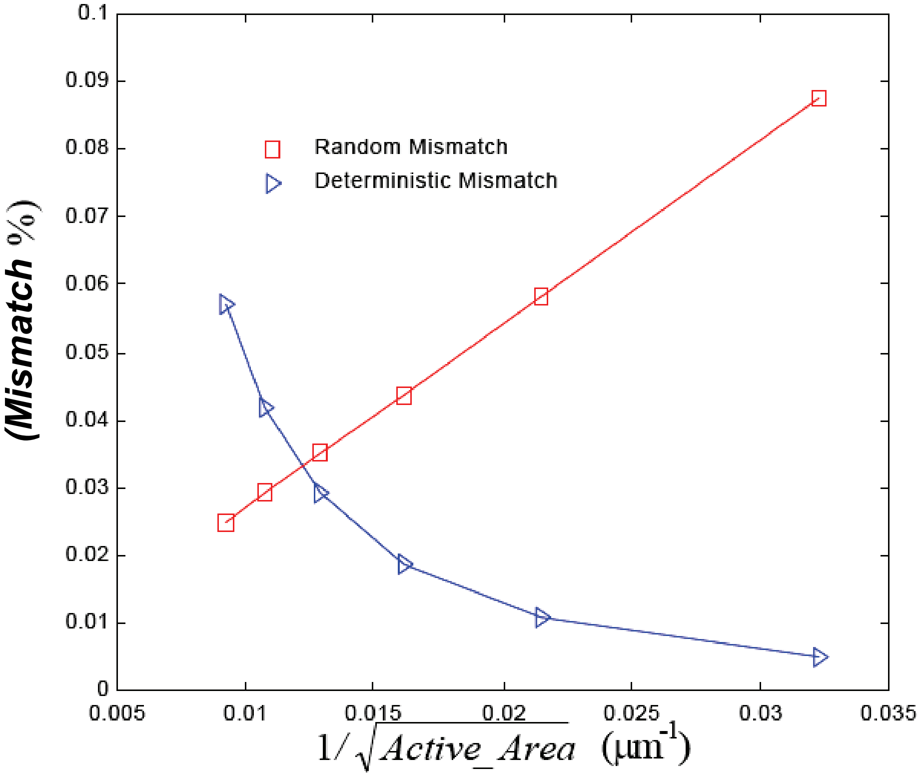


$$Mismatch = \frac{I_{D2} - I_{D1}}{I_{D1}} x100 \ \%$$

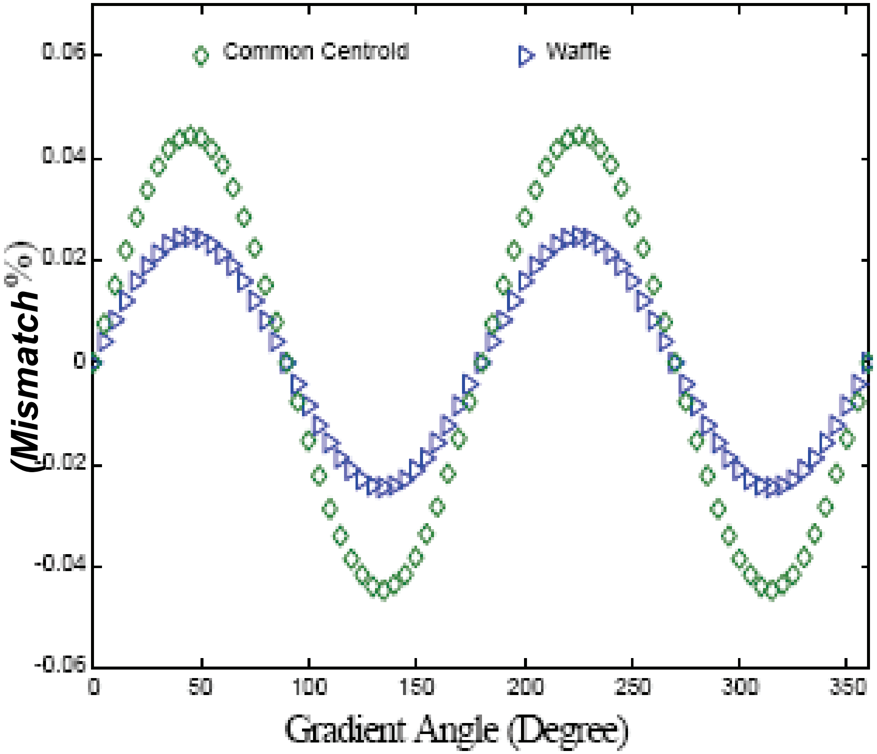
Reduction of mismatch (linear gradient consideration)

Waffle Layout Structure





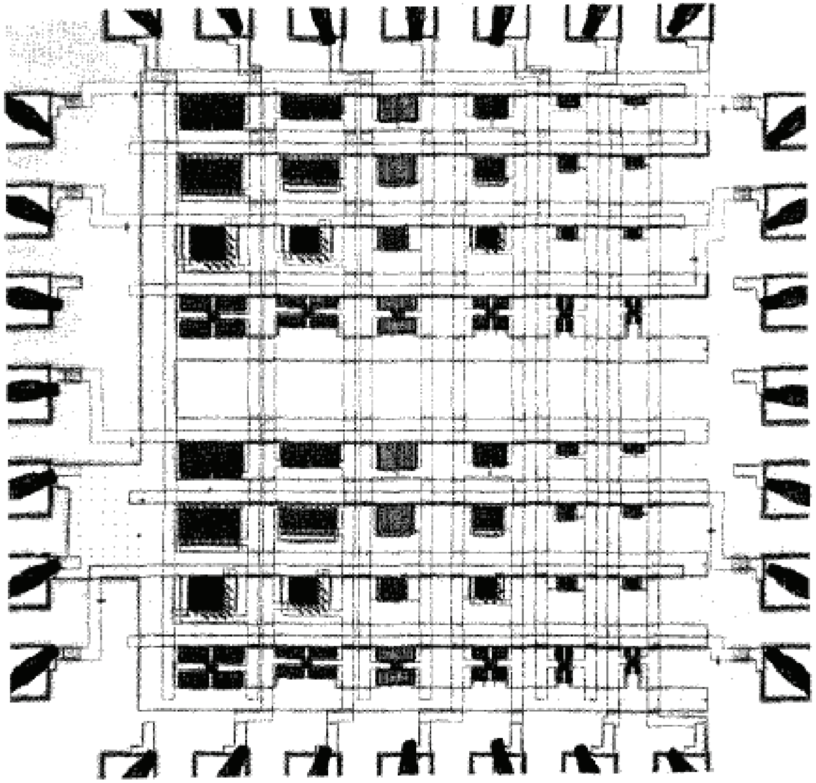
Deterministic and Random Mismatches of Waffle Structure



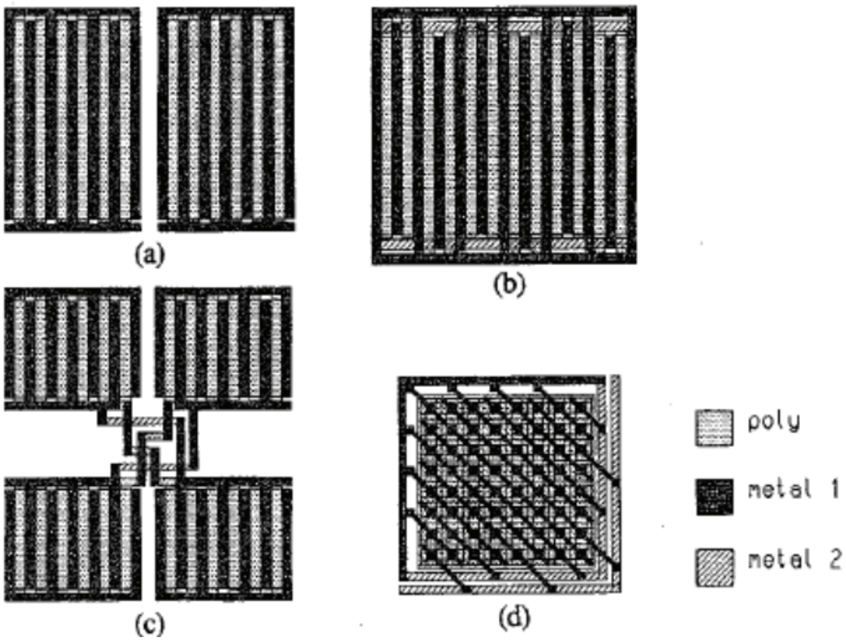
Mismatch of Common Centroid and Waffle Structure

Reduction of mismatch (linear gradient consideration)

Test structures for mismatch characterization of most common structures



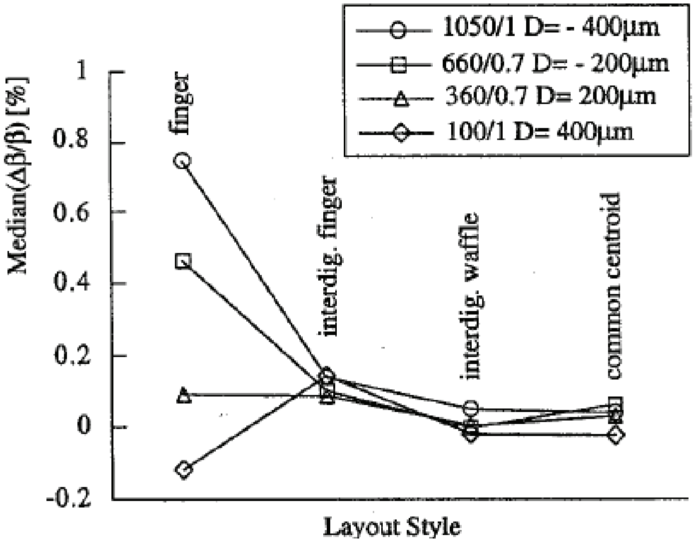
Microphotograph of test chip



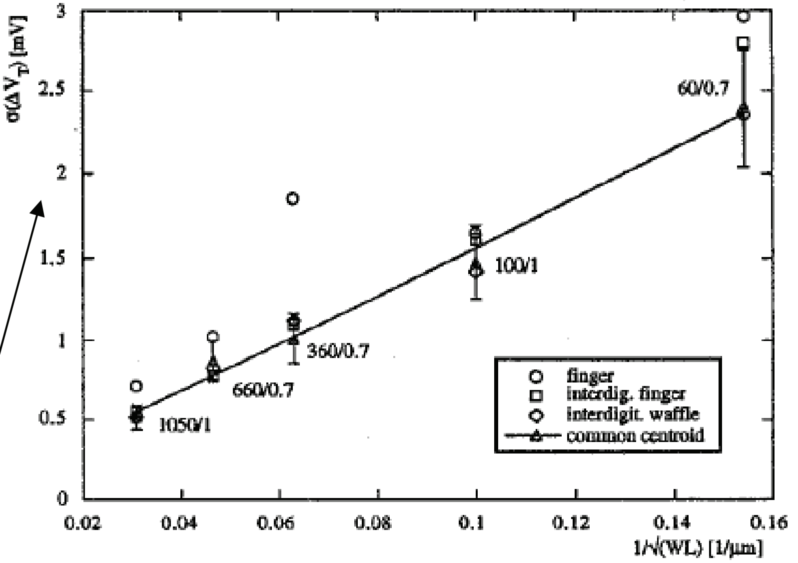
Layout styles:
(a) Finger (siimple technique).
(b) interdigitated finger.
(c) Quad (common centroid technique).
(d) interdigitated waffle.

Reduction of mismatch (linear gradient consideration)

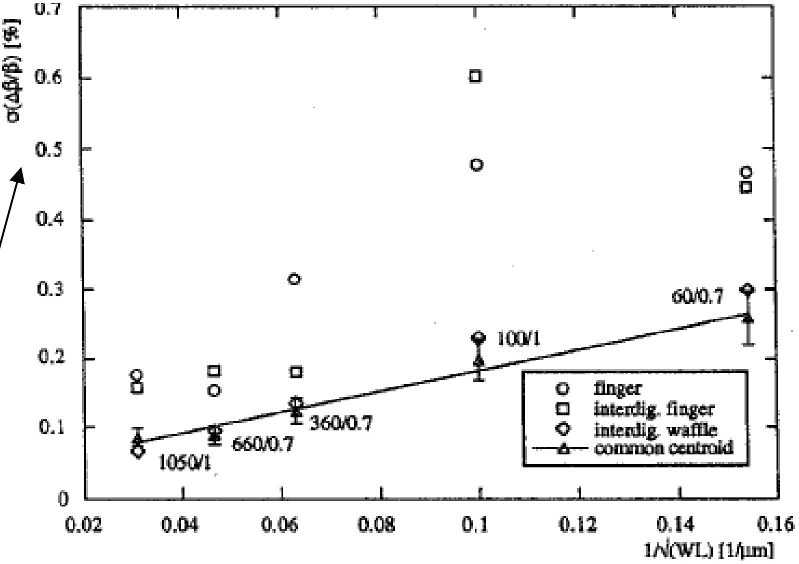
Mismatch characterization results for most common structures



Median of the relative β mismatch values. D-relative distance from the die center, in the x direction.



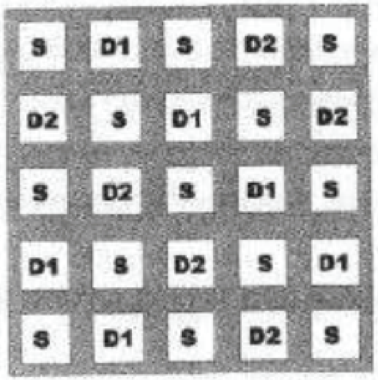
Standard deviation of VT mismatch versus the inverse transistor area



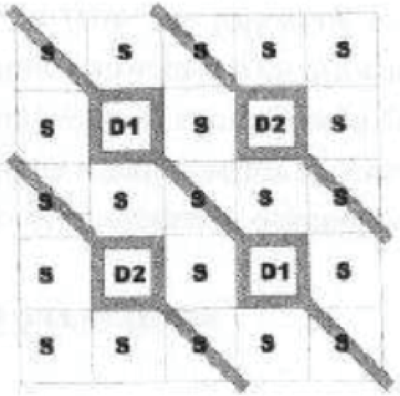
Standard deviation of relative β mismatch versus the inverse transistor area

Reduction of mismatch (linear gradient consideration)

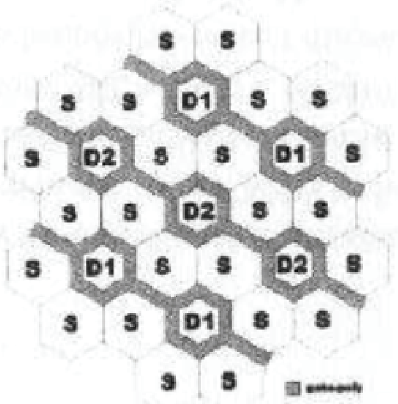
Hexagonal structure



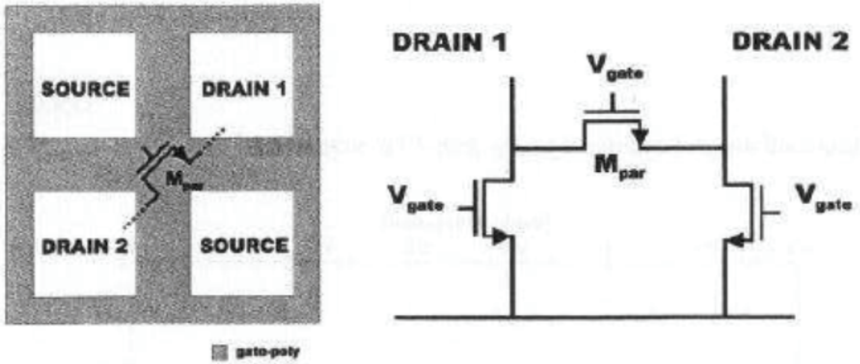
Interdigitated waffle



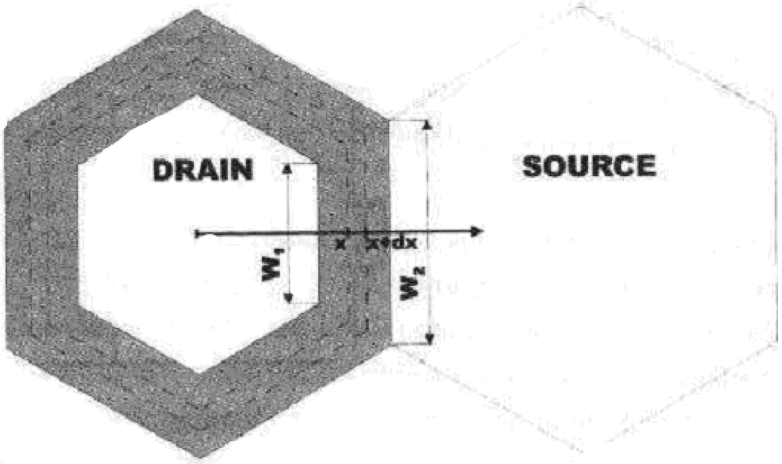
Square structure



Hexagonal structure



Parasitic transistor created by the interdigitated waffle structure

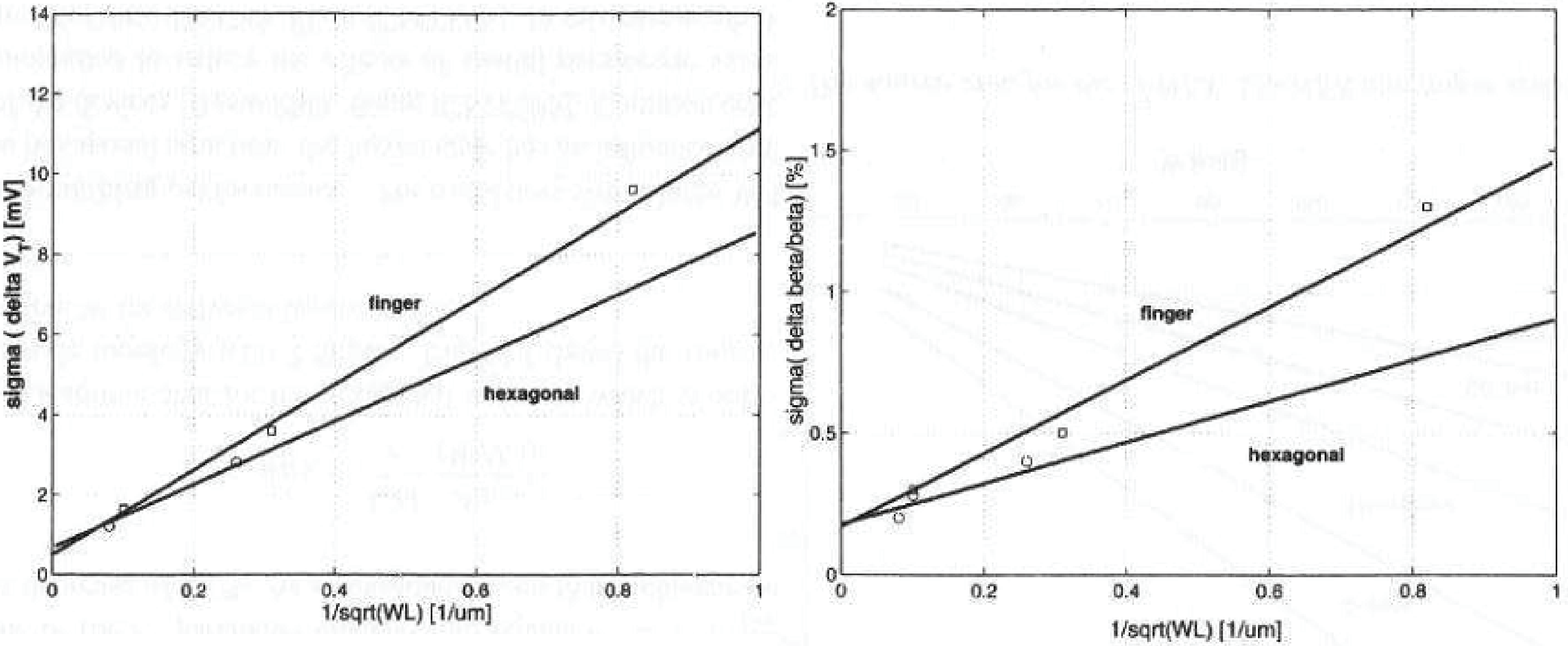


Effective W/L ratio Calculation for hexagonal structure:

$$\left(\frac{W}{L}\right)_{eff} = \frac{8}{\ln\left(\frac{W_2}{W_1}\right)}$$

Reduction of mismatch (linear gradient consideration)

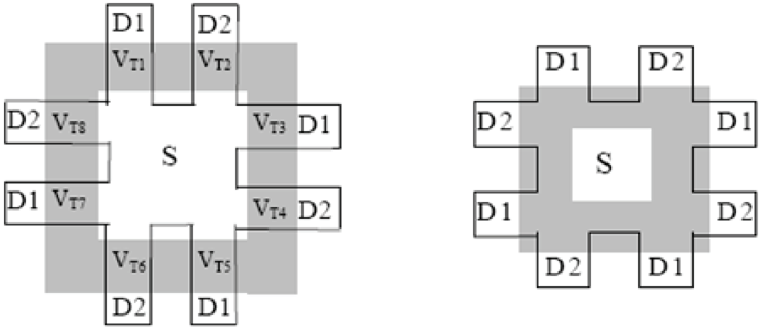
Matching behavior of hexagonal structure compared to finger structure:



Reduction of mismatch (linear gradient consideration)

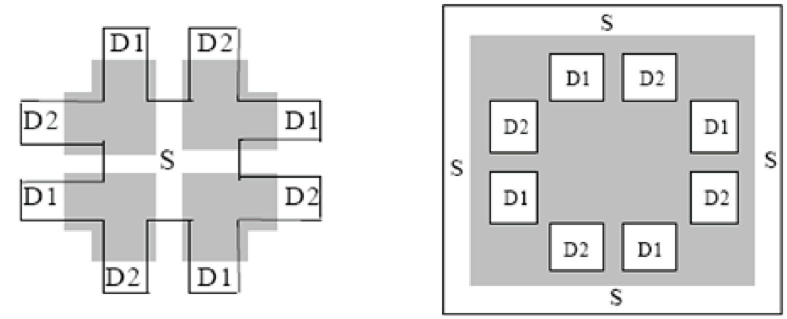
Segmented structures

(common source diffusion, segments are placed at right angles)



(a) Type I

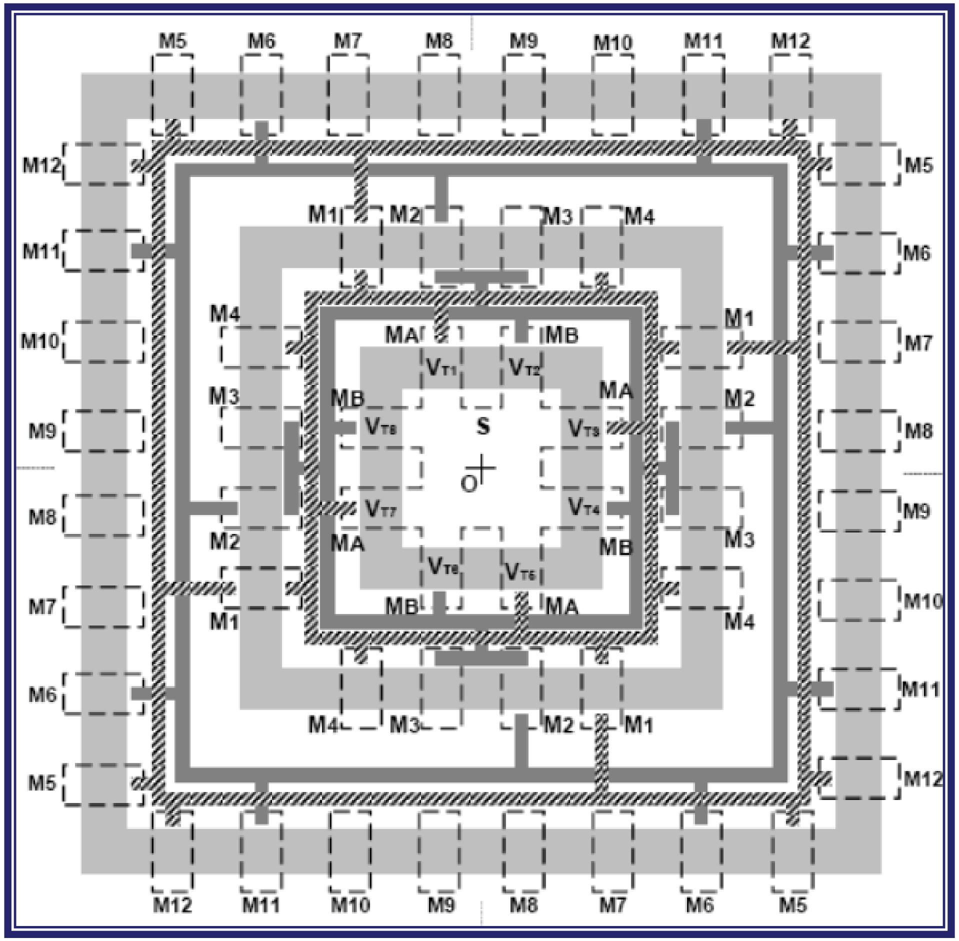
(b) Type II



(c) Type III

(d) Type IV

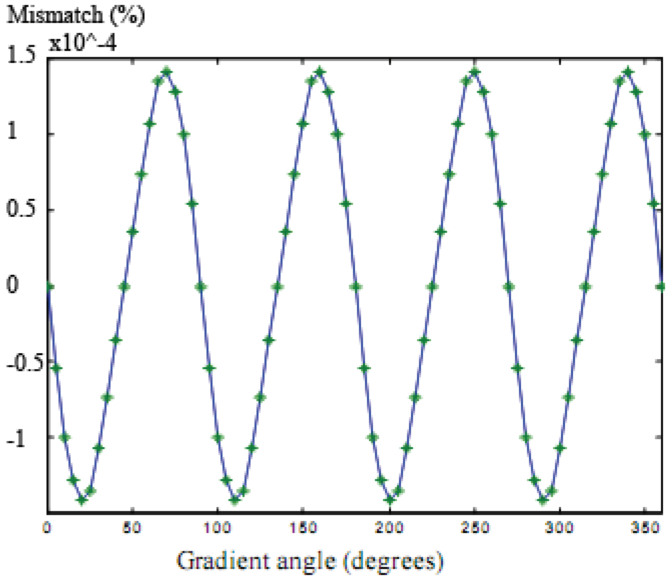
Matching enhanced current mirror layout techniques



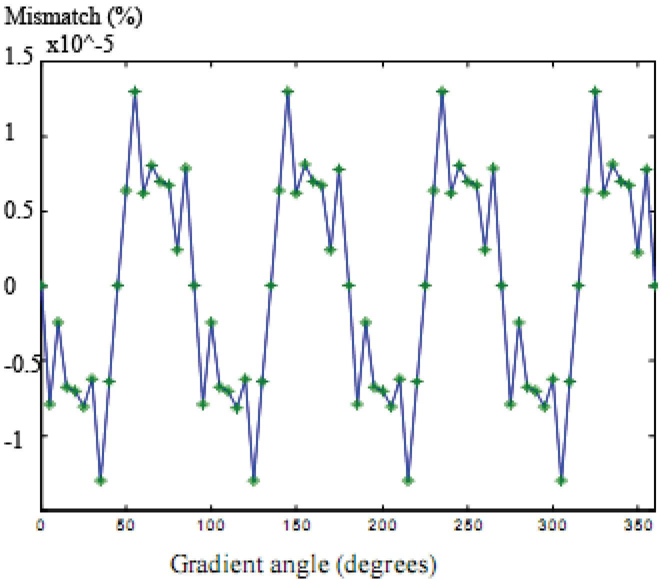
Example of practical Four-segment rectangular structure (Type I) for eight cascode current sources

Simulation results of segmented structures of Type I - IV

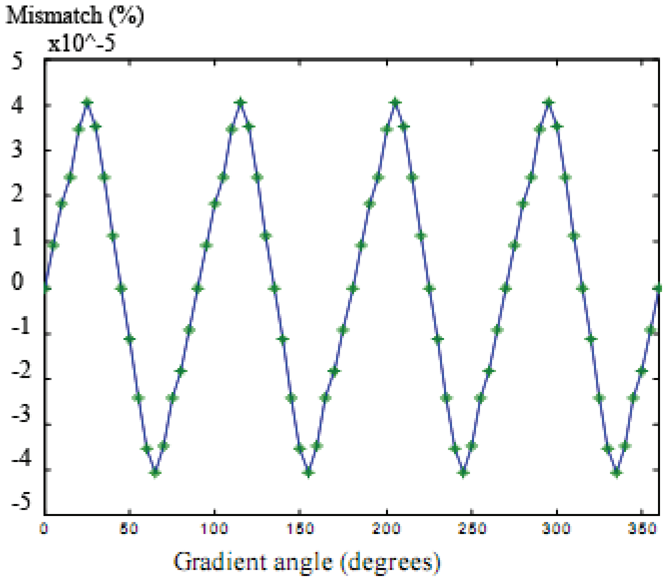
(a)



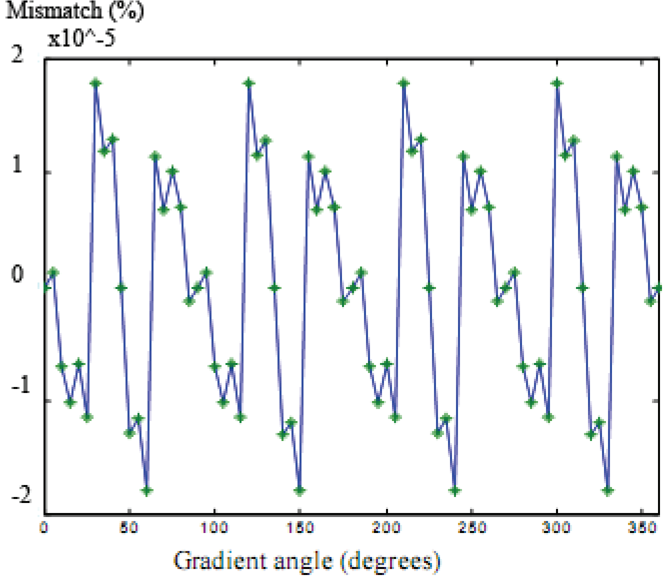
(b)



(c)

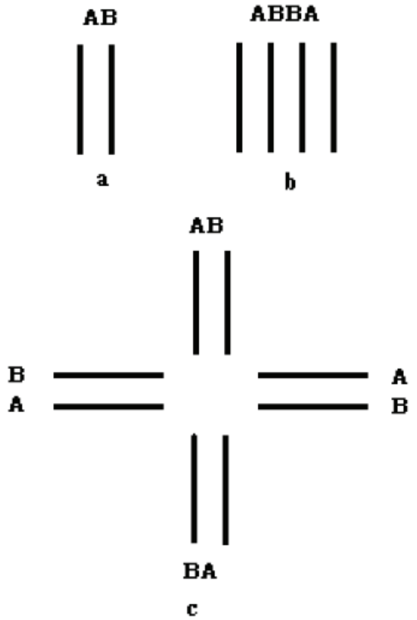


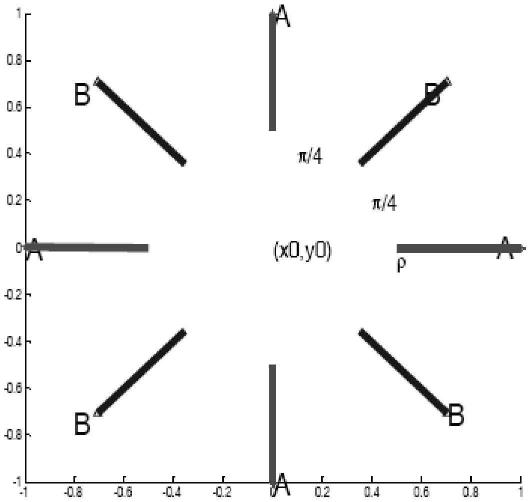
(d)



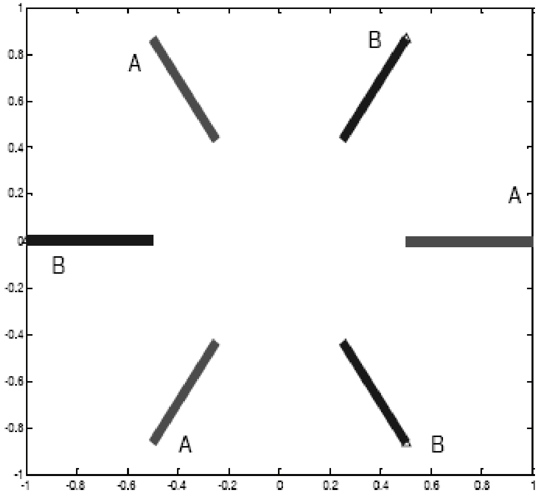
Reduction of mismatch (nonlinear gradient consideration)

Circular symmetry structures





2nd order circular symmetry pattern



Hexagonal Tessellation

Existing Layout Patterns:

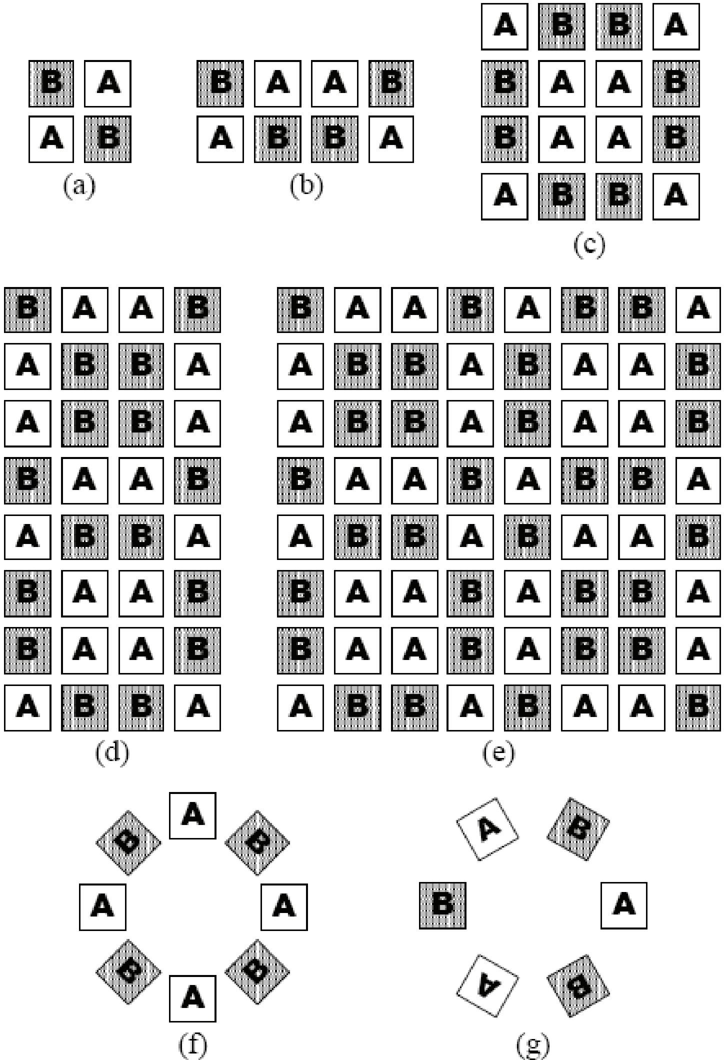
- *(a)* ***- simple;***
- *(b)* ***- common centroid (interdigitized);***
- *(c)* ***- Four segment.***

Simulation comparison between different layout patterns:

Layout structure	Worst mismatch(%)
Simple	4.8807
Common centriod	1.6966e-2
Four segment	1.4090e-4
2nd order circular symmetric	0
hexagonal tessellation	0

Reduction of mismatch (nonlinear gradient consideration)

Comparison of common-centroid based and circular symmetry patterns


(a)

```
B A
A B
```

(b)

```
B A A B
A B B A
```

(c)

```
A B B A
B A A B
B A A B
A B B A
```

(d)

```
B A A B
A B B A
A B B A
B A A B
A B B A
B A A B
B A A B
A B B A
```

(e)

```
B A A B A B B A
A B B A B A A B
A B B A B A A B
B A A B A B B A
A B B A B A A B
B A A B A B B A
B A A B A B B A
A B B A B A A B
```

(f)

(g)

Simulation results for systematic mismatch

Mismatch (%)	Highest Order of Gradient Effect				
	1st	2nd	3rd	4th	5th
Fig. (a)	0	2.77	5.22	7.43	10.39
Fig. (b)	0	0	0.24	0.87	1.70
Fig. (c)	0	0	0	0.01	0.068
Fig. (d)	0	0	0	0	0.0023
Fig. (e)	0	0	0	0	0
Fig. (f)	0	0	0	0.026	0.18
Fig. (g)	0	0	0.26	0.50	2.24

Layout structures for Nonlinear Gradient Cancellation: 1st order (common centroid) - 5th order central symmetrical patterns (a) - (e), 2nd order circular symmetry pattern (f) and hexagonal tessellation (g).

Measurements of more than 100 chips show that the 2nd-order central symmetry pattern has less than 0.04% and the 3rd-order has less than 0.002% systematic mismatch errors.

Layout techniques for improved matching: Conclusions

- Segmented structures are predicted to have better linear gradient cancellation than common centroid
- Hexagonal tesselation is predicted to cancel up to 2nd order gradient
- Common-centroid based patterns organized in a special way are predicted to cancel higher order gradients

Conclusions:

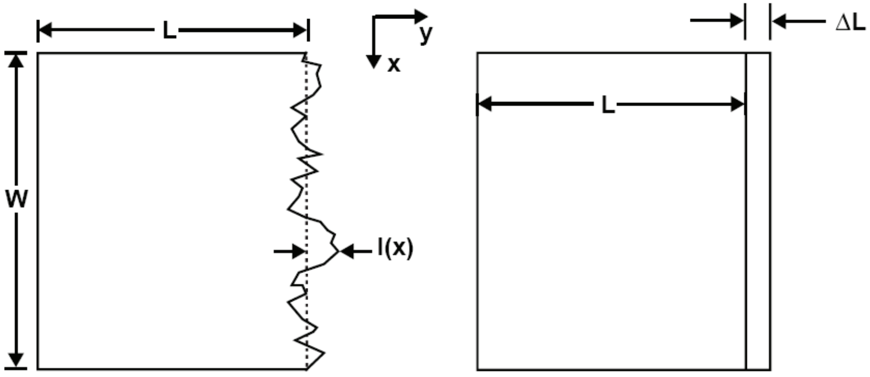
- Analysis of drain current mismatch is based on the basic current mirrors.
- Represented models for simulation of random and systematic mismatch are consistent and consume not much machine time.
- Total mismatch modeling should include both random and systematic mismatch components.
- Segmented structures with common source diffusion and segments placed at right angles, hexagonal tessellation, 2nd order circular symmetry and common-centroid based patterns are predicted to have best matching characteristics.
- Prospectives:
  - Models need to include more parameters that influence mismatch for higher accuracy.
  - Layout structure of multiple combined hexagonal tessellations should be analyzed.
- The presented review is based on more than 60 scientific sources up to 2009 year.

Thank You for your attention

Random mismatch

- Sources for **local mismatch**:
  - polysilicon or metal grain edge boundaries,
  - local etch variation,
  - local implant or diffusion variations.
  - variations in gate oxide thickness or permittivity,
  - dopant variations.

- Sources for **global mismatch**:
  - line edge variation,
  - stepper lens aberrations,
  - loading effects,
  - optical proximity shifts.

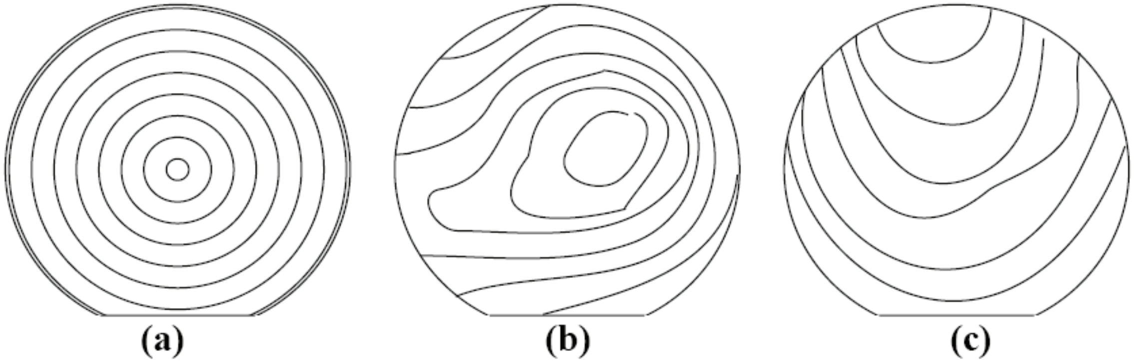


(a) Local Mismatch (b) Global Mismatch

A comparison of local and global mismatch errors

Systematic mismatch:

- Results from gradients in processing, stress, and temperature.
- Wafer processing gradients:
  - ☐ radially based gradients *(photoresist coat, development, hot-plate bakes, plasma etch, etc.)*;
  - ☐ monotonic gradients.
- Process gradients may be radial, linear or otherwise spatially dependent, but given the proximity of devices in a matching pair, it is reasonable to **consider all gradients to be linear**



Radially based wafer gradients