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Sigma-Delta data converters architectures comparison

Traditional data converters sample input signal at Nyquist frequency (and this is their virtue). They are often difficult to implement in fine-line very large scale integration technology (VLSI). This difficulties arise because conventional methods need precise analog components in their filters and conversion circuits and because their circuits can be very vulnerable to noise and interference. Also they cannot provide necessary resolution because of approximately doubling chip area with increasing resolution for every bit. Some algorithms or calibration methods must be used to achieve necessary characteristics. But still remains the problem of noise shaping.

Method of data conversion that solve both problems is sigma-delta modulation – a method of encoding signals using pulse-density modulation. Oversampling converters can use simple and relatively high-tolerance analog components to achieve high resolution but they require fast and complex digital signal processing stages. The design of sigma-delta modulators can trade resolution in time for resolution in amplitude in such way that imprecise analog components can be tolerated.

The first-order sigma-delta modulator feeds the input signal to the quantizer via an integrator, and the quantized output feeds back to subtract from the input signal. This feedback forces the average value of the quantized signal to track the average input. Any persistent difference between them accumulates in the integrator and eventually corrects itself. Higher-order modulators show higher signal-to-noise ratio, but the problem of instability and overflow exists. Therefore other architectures can be used.

Using delta-sigma modulators today is the best way to design high-resolution compact DAC or ADC. With growth of OSR and complexity of modulator SNR grows too. The choice of the architecture must be a tradeoff between the OSR and complexity of architecture. With OSR greater then 256 it will be difficult to work with high-frequency signals and to implement an output filter. Using error-feedback or cascade architecture shows best result – 60.3 dB of SNR at OSR of 256. Care must be taken while designing analog part of converters, because mismatches in components will introduce high distortion into signal being converted. To compare SD converters architectures by SNR (ENOB) a Matlab model was developed. The SNR data derived by Matlab simulation for different modulators with different oversampling ratios is shown in table 1.

Table 1. SNR and ENOB for different modulator structures and OSR

Architecture	SNR (dB) (ENOB)			
	64	128	256	512
First-order	22.3 (3.41)	25.4 (3.93)	38.3 (6.07)	43.3 (6.89)
Second-order	20.8 (3.16)	32.6 (5.12)	39.4 (6.26)	52.5 (8.38)
Error-feedback	42.8 (6.81)	56.4 (9.08)	60.3 (9.73)	83.2 (13.53)
Error-feedback 2nd order	36.5 (5.78)	48.1 (7.69)	55.1 (8.87)	85.5 (13.92)
Cascade	42.8 (6.81)	56.4 (9.08)	60.3 (9.73)	83.3 (13.54)
Cascade1-2	42.8 (6.81)	56.4 (9.08)	60.3 (9.73)	83.3 (13.54)

The data obtained by simulation allows to choose architecture and OSR suitable for particular application.

References

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