METHODS OF DESIGNING ANALOG-TO-DIGITAL CONVERTERS

Master’s Thesis Presentation

Author: Olena Shvaichenko
Purpose

The purpose is to investigate the design of 14-bit resolution ADC with sampling frequency 2 MHz in 0.13 um technology.
# ADC architectures

## Comparison table

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Speed</th>
<th>Conversion time</th>
<th>Resolution</th>
<th>Area</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash ADC</td>
<td>High</td>
<td>Constant</td>
<td>Low (up till 8 bits)</td>
<td>Increases exponentially with resolution</td>
<td>Very high</td>
</tr>
<tr>
<td>Pipelined ADC</td>
<td>Medium-high</td>
<td>Increases with resolution</td>
<td>Medium-high (up till 12-bits)</td>
<td>Increases linearly with resolution</td>
<td>Medium</td>
</tr>
<tr>
<td>Sigma-Delta ADC</td>
<td>Medium</td>
<td>Trade off with resolution</td>
<td>High (up till 24-bits)</td>
<td>Constant; no change with increase in resolution</td>
<td>Medium-low</td>
</tr>
<tr>
<td>SAR ADC</td>
<td>Medium-low</td>
<td>Increases with resolution</td>
<td>High (up till 18-bits)</td>
<td>Increases linearly with resolution</td>
<td>Medium-low</td>
</tr>
</tbody>
</table>

## Spec

- **Resolution**
  - 14 bit
- **Frequency**
  - 2 MHz
- **Technology**
  - SG13S
- **Power supply**
  - 1.2 V

---

Spec

Resolution

- 14 bit

Frequency

- 2 MHz

Technology

- SG13S

Power supply

- 1.2 V
Successive approximation ADC

Advantages
• Low power consumption,
• Low circuit complexity
• Mostly digital circuitry.

Limitations
• Lower sampling rates
• Accuracy of the system depends on the accuracy of the DAC and the comparator.
Successive approximation ADC

Principle of operation

\[ V_{in} = b_1 \frac{V_{REF}}{2} + b_2 \frac{V_{REF}}{4} + b_3 \frac{V_{REF}}{8} + b_4 \frac{V_{REF}}{16} \]
Mathematical model
Mathematical model

**Imperfections**
- Offset voltage
- Jitter
- Thermal noise
- Settling time limitations
- Clock feedthrough
- Parasitic capacitance

**Mismatches**
- Offset voltage
- Settling time limitations
- Parasitic capacitance

- **ramp**
  - >10 samples per transition level
- **sine-wave**
  - coherent sampling

- **Input**
  - SAR ADC
- **Output**
  - Ideal DAC

- **Histogram method**
- **FFT**

**Static:**
- Gain error, Offset, INL, DNL.

**Dynamic:**
- THD, SFDR, SINAD, ENOB.
Modeling of Capacitor array mismatch effect

Pelgrom’s Law:

$$\delta \left( \frac{\Delta C}{C} \right) = \frac{K_p}{\sqrt{WL}}$$

$K_p$ - is matching parameter

Common centroid structure

$$C_i = 2^{i-1}C_1, \ i = 1, N$$

$$\delta_{C_i} = \frac{\delta_{C_1}}{\sqrt{2^{i-1}}}$$
Simulation results of modeling Capacitor array mismatch effect

Mismatch → Cu = 6.5 fF
Modeling of Settling time effect

**Sampling phase**

\[ V_h = V_{in}(1 - e^{-\frac{t_{clk}}{\tau}}) \]

\[ t_{clk} = \frac{1}{N_{cycles}f_s} \Rightarrow \tau = R_{sw eq}C_{tot} \]

\[ R_{sw} = \frac{1}{C_{ox\mu_{eff}}W/L(V_{GS} - V_t)} \]

**Sampling frequency → Switches sizing.**
Behavioural model

Differential triple reference charge-redistribution SAR ADC with monotonic switching procedure

Reduces Ctot by a factor of 4 compared to conventional
Behavioural model test bench
Simulation results of behavioral model
Simulation results of behavioral model
Transistor level model

Comparator architecture

![Comparator architecture diagram]
Comparator schematic
Simulation results

Input and output waveforms

Transient Response

- yin
- yout
- yout
- yin

0.0 25.0 50.0 75.0 100.0

time (ns)
Conclusion

✓ Analysis of ADC architectures was done.
✓ SAR architecture was chosen as most appropriate architecture to meet given specification.
✓ Development of program for modeling successive-approximation analog-to-digital conversion in MATLAB was done.
✓ Analysis of non-ideal effects in SAR ADC was done.
✓ Modeling of mismatch, input referred dc offset and settling time effects was done.
✓ Simulation of modeling mismatch effect shows that for SG013S IHP technology it is possible to get $DNL \leq 0.5$ LSB, $INL < 0.5$ LSB, $THD = -95.07$ dB, $SFDR = 85.75$ dB, $SINAD = 84.84$ dB, $ENOB = 13.8$ bit with probability 99.7%.
✓ Simulation of modeling comparator offset voltage effect shows that for SG013S IHP technology with 3.2 mV input referred dc offset it is possible to get $THD = -84.33$ dB, $SFDR = 76.10$ dB, $SINAD = 74.95$ dB, $ENOB = 12.16$ bit with probability 99.7%.
Conclusion

✓ Simulation of modeling settling time effect shows that for SG013S IHP technology with 2.1 ns time constant it is possible to get SFDR = 83.97 dB, SINAD = 83.7 dB, ENOB = 13.61 bit with probability 99.7%.

✓ Verilog–A behavioral model of 14-bit differential charge–redistribution SAR ADC with monotonic switching procedure was developed.

✓ Simulation of proposed high-speed comparator with resolution 40μV, clock frequency 100 MHz, supply voltage 1.2 V in SG013S IHP technology was done.

✓ Analysis of more than 45 scientific sources up to 2011 year in the field of analog-to-digital conversion has been conducted.

Results of investigation have been published at the International conference on system analysis and information technologies.

The investigation was carried out for IHP - Innovations for High Performance Microelectronics company.
Thank You!!!
General concept in designing ADC

Design flow for ADC

• Mathematical model
  • Algorithm is examined
  • Functional description

• Behavioural model
  • Architecture is verified
  • Behavioural description of the blocks

• Transistor level model
  • Schematic is verified
  • Transistor level of the blocks

• Layout level

Abstract model in Matlab, C/C++

Verilog/VHDL model of the digital part;
Verilog-A/VHDL-AMS model for the analog

Synthesis to get gate level Verilog or VHDL
Schematic design of the analog
Mixed verification
Analog layout
Place&Rout of the digital
Post-layout simulation
Modeling of Capacitor array mismatch effect

If standard deviation of unit capacitance is defined as

\[ s_{C_1} = s \left( \frac{\Delta C_1}{C_1} \right) = \frac{K_p}{\sqrt{W_1 L_1}} \]

\[ s(\Delta C_1) = C_1 s_{C_1} \]

The next capacitor will be parallel connection of 2 unit capacitor and it’s mismatch will be the sum of unit capacitor mismatches. Since this mismatches are independent random variables with Gaussian distributions, the standard deviations can be related as follows.

\[ s(\Delta C_2) = \sqrt{\left( C_1 s_{C_1} \right)^2 + \left( C_1 s_{C_1} \right)^2} = C_1 s_{C_1} \sqrt{2} \]

\[ s_{C_2} = s \left( \frac{\Delta C_2}{C_2} \right) = \frac{C_1 s_{C_1} \sqrt{2}}{C_2} = \frac{C_1 s_{C_1} \sqrt{2}}{2C_1} = \frac{s_{C_1}}{\sqrt{2}} \]

Thus for

\[ C_i = 2^{i-1} C_1 \]

\[ s_{C_i} = \frac{s_{C_1}}{\sqrt{2^{i-1}}} \]
Simulation results of modeling
Settling time effect

THD = -98.90 dB
TSD = -86.98 dB
SFDR = 83.97 dB
SINAD = 83.70 dB
ENOB = 13.61 bits

Power spectral density

ADC with $\tau = 2.1$ ns
Waveforms of conventional and monotonic switching procedure
Waveforms of conventional and monotonic switching procedure

Waveform of conventional switching procedure

Waveform of monotonic switching procedure

Reduces Switching power in a factor of 5
Preamplifiers

- Preamplifier with diode connected pMOS load and it’s gain
- Preamplifier with resistor load and it’s gain
- Modified Bult’s preamplifier and it’s gain
- Song’s preamplifier and it’s gain
# Transistor level model

## Preamplifier

<table>
<thead>
<tr>
<th>Amplifier architecture</th>
<th>Gain, dB</th>
<th>Bandwidth, Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential pair with resistive load</td>
<td>13.88</td>
<td>565.7</td>
</tr>
<tr>
<td>Differential pair with pmos diode connected load</td>
<td>4.86</td>
<td>465.2</td>
</tr>
<tr>
<td>Modified Built’s preamplifier</td>
<td>20.13</td>
<td>201.3</td>
</tr>
<tr>
<td>Song’s preamplifier</td>
<td>20.42</td>
<td>178.1</td>
</tr>
</tbody>
</table>
Transistor level model

Latch

Dynamic latch

Advantages

- Zero dc current in reset mode,
- Full logic levels after regeneration,
- Outputs are both reset to supply voltage so they are well defined.