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Review of device matching improvement methods in integrated circuits

This paper provides a wide review of the work conducted in the field of device matching improvement methods in integrated circuits up to 2009 year. More than 50 scientific sources have been analyzed.

Due to the influence of many unavoidable factors including process variation and environment difference, present manufacturing technologies are still unable to produce devices without mismatch problems. These component mismatches destroy the performance of high accuracy integrated circuits. A simple current mirror usually requires two perfectly matched transistors, but there is always some mismatch between these two transistors after fabrication and the circuit performance will be degraded seriously. A good understanding of the matching behavior of components available in a particular integrated circuit technology is critical in designing analog IC's. With the advances in technology leading to smaller feature sizes and more stringent design constraints, device mismatch considerations are becoming increasingly important.

The analysis of existing layout techniques, methods of modeling and characterization have been conducted. The classification of the existing solutions have been done considering ways of improving matching characteristics for transistors and devices, linear and nonlinear gradient cancellation, common centroid, interdigitized, waffle, segmented layout techniques. Analytical and numerical models for mismatch simulations, that describe random and systematic mismatch, linear and nonlinear gradients, schematic parameters' variations, consider distance between devices, their sizes and rotation, are represented. Also analysis of papers on characterization of mismatch in current mirrors, DACs and separate transistors is done.

In [1] the comparison of common centroid, interdigitized, waffle and segmented layout techniques for current mirrors with computer simulations for threshold voltage gradients at all angles across the active area is conducted. This subject is extended and the layout for four (8, 16, etc.) cascode current sources is proposed in [2]. The purpose of such layouts is to reduce the matching sensitivity to linear parameter gradients in high performance integrated circuit applications. Techniques, that allow cancellation of the mismatch between two devices due to nonlinear gradient up to n^{th} order by using 2^n unit cells for each device, are presented in [3].

Based on statistical methods analytical models for threshold voltage and current factor that relate the mismatch to the device dimensions are developed in [4]. The analysis and measurements of the mismatch in threshold voltage, current factor and the substrate factor of the MOS transistor as a function of area, distance and orientation are conducted in [5].

References

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